



Data Sheet

$\pi 120M1/\pi 122M1$

FEATURES

Ultra low power consumption (1Mbps):

0.58mA/Channel

High data rate:

$\pi 12xM1x$: 10Mbps

High common-mode transient immunity: 75 kV/ μs typical

High robustness to radiated and conducted noise

Low propagation delay:

8 ns typical for 5 V operation

9 ns typical for 3.3 V operation

Isolation voltages:

$\pi 12xM1x$: AC 1500Vrms

High ESD rating:

ESDA/JEDEC JS-001-2017

Human body model (HBM) $\pm 8kV$, all pins

3 V to 5.5 V level translation

Wide temperature range: $-40^{\circ}C$ to $125^{\circ}C$

8-PIN, RoHS-compliant, DFN package(3mm*2mm)

APPLICATIONS

General-purpose multichannel isolation

Industrial field bus isolation

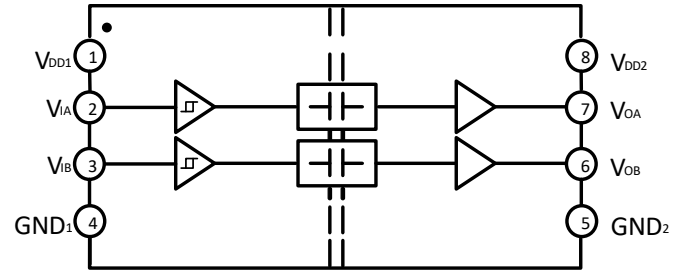
GENERAL DESCRIPTION

The $\pi 1xxxxx$ is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using matured standard semiconductor CMOS technology and 2PaiSEMI *iDivider* technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

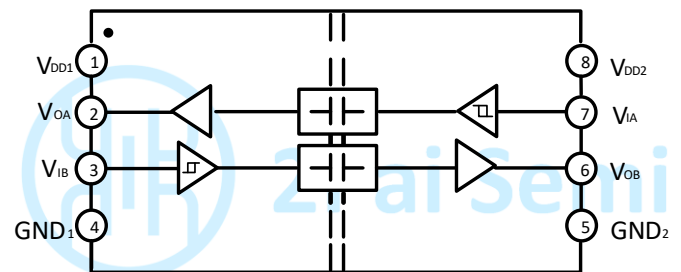
Intelligent voltage divider technology (*iDivider* technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The $\pi 1xxxxx$ isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS



(a) $\pi 120M1x$



(b) $\pi 122M1x$

Figure1. $\pi 120M1x/\pi 122M1x$ functional Block Diagram

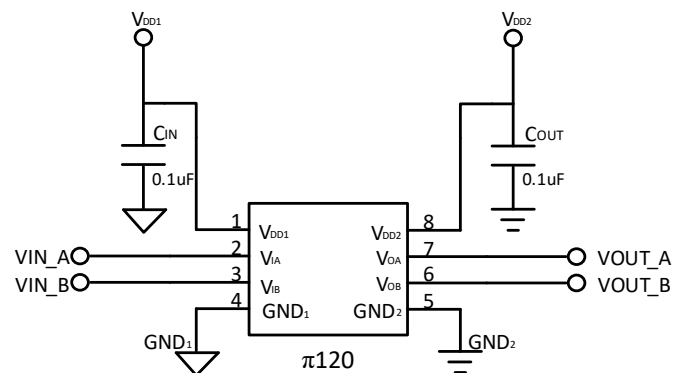


Figure2. $\pi 120M1x$ Typical Application Circuit

Rev.1

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PIN CONFIGURATIONS AND FUNCTIONS

π 120M1x Pin Function Descriptions

Pin No.	Name	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND ₂	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

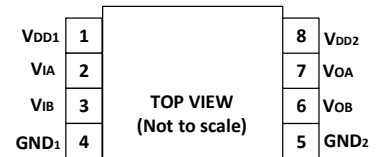


Figure3. π 120M1x Pin Configuration

π 122M1x Pin Function Descriptions

Pin No.	Name	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{OA}	Logic Output A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND ₂	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{IA}	Logic Input A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

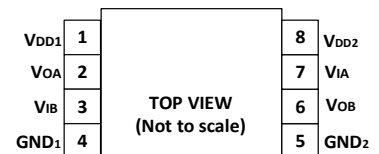


Figure4. π 122M1x Pin Configuration

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 1. Absolute Maximum Ratings³

Parameter	Rating
Supply Voltages (V _{DD1} -GND ₁ , V _{DD2} -GND ₂)	-0.5 V to +7.0 V
Input Voltages (V _{IA} , V _{IB}) ¹	-0.5 V to V _{DDx} + 0.5 V
Output Voltages (V _{OA} , V _{OB}) ¹	-0.5 V to V _{DDx} + 0.5 V
Average Output Current per Pin Side 1 Output Current (I _{O1})	-10 mA to +10 mA
Average Output Current per Pin Side 2 Output Current (I _{O2})	-10 mA to +10 mA
Common-Mode Transients Immunity ²	-150 kV/μs to +150 kV/μs
Storage Temperature (T _{ST}) Range	-65°C to +150°C
Ambient Operating Temperature (T _A) Range	-40°C to +125°C

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

² See Figure13 for Common-mode transient immunity (CMTI) measurement.

³ Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx}^1	3		5.5	V
High Level Input Signal Voltage	V_{IH}	$0.7 \cdot V_{DDx}^1$		V_{DDx}^1	V
Low Level Input Signal Voltage	V_{IL}	0		$0.3 \cdot V_{DDx}^1$	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Maximum Data Rate		0		10	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .

Truth Tables

Table 3. $\pi 120M1x/\pi 122M1x$ Truth Table

V_{ix} Input ¹	V_{DDI} State ¹	V_{DDO} State ¹	Default Low V_{Ox} Output ¹	Default High V_{Ox} Output ¹	Test Conditions /Comments
Low	Powered ²	Powered ²	Low	Low	Normal operation
High	Powered ²	Powered ²	High	High	Normal operation
Open	Powered ²	Powered ²	Low	High	Default output
Don't Care ⁴	Unpowered ³	Powered ²	Low	High	Default output ⁵
Don't Care ⁴	Powered ²	Unpowered ³	High Impedance	High Impedance	

Notes:

¹ V_{ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

² Powered means $V_{DDx} \geq 2.9$ V

³ Unpowered means $V_{DDx} < 2.3$ V

⁴ Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DDI} through its ESD protection circuitry.

⁵ If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1 μ s. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 1 μ s.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 4. Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			100	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		10			Mbps	Within PWD limit
Propagation Delay Time ¹	t_{pHL}, t_{pLH}	5.5	8	12.5	ns	The different time between 50% input signal to 50% output signal @ $5V_{DC}$ supply
		6.5	9	13.5	ns	@ $3.3V_{DC}$ supply
Pulse Width Distortion	PWD	0	0.3	0.8	ns	The max different time between t_{pHL} and t_{pLH} @ $5V_{DC}$ supply. And The value is $ t_{pHL} - t_{pLH} $
		0	0.3	0.8	ns	@ $3.3V_{DC}$ supply

Channel to Channel Propagation Delay Skew	t_{CSK}	1.5	0	0.8	ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply. @ 3.3V _{DC} supply
			0	1	ns	
Output Signal Rise/Fall Time	t_r/t_f		1.5		ns	10% to 90% signal terminated 1MΩ/14pF oscilloscope input impedance, See figure10.
Rated Dielectric Insulation Voltage	V _{ISO}	1.5			kV rms	1-minute duration
Common-Mode Transient Immunity ³	CMTI		75		kV/μs	V _{IN} = V _{DDx} ² or 0V, V _{CM} = 1000 V.
ESD (HBM - Human body model)	ESD		±8		kV	All pins

Notes:

¹ t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See figure 16.² V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.³ See Figure13 for Common-mode transient immunity (CMTI) measurement.**Table 5. DC Specifications**V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V _{IT+}		0.6*V _{DDx} ¹	0.7*V _{DDx} ¹	V	
Falling Input Signal Voltage Threshold	V _{IT-}	0.3* V _{DDx} ¹	0.4* V _{DDx} ¹		V	
High Level Output Voltage	V _{OH} ¹	V _{DDx} - 0.1	V _{DDx}		V	-20 μA output current
		V _{DDx} - 0.2	V _{DDx} - 0.1		V	-2 mA output current
Low Level Output Voltage	V _{OL}	0	0.1	0.1	V	20 μA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I _{IN}	-10	0.5	10	μA	0 V ≤ Signal voltage ≤ V _{DDx} ¹
V _{DDx} ¹ Undervoltage Rising Threshold	V _{DDxUV+}	2.45	2.65	2.9	V	
V _{DDx} ¹ Undervoltage Falling Threshold	V _{DDxUV-}	2.3	2.5	2.75	V	
V _{DDx} ¹ Hysteresis	V _{DDxUVH}		0.15		V	

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.**Table 6. Quiescent Supply Current**V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	
π120M1x Quiescent Supply Current @ 5V _{DC} Supply	I _{DD1} (Q)	64	80	104	μA	0V Input signal	
	I _{DD2} (Q)	781	976	1269	μA	0V Input signal	
	I _{DD1} (Q)	158	197	256	μA	5V Input signal	
	I _{DD2} (Q)	738	923	1200	μA	5V Input signal	
	@ 3.3V _{DC} Supply	I _{DD1} (Q)	63	79	103	μA	0V Input signal
		I _{DD2} (Q)	772	965	1255	μA	0V Input signal
		I _{DD1} (Q)	116	145	189	μA	3.3V Input signal
		I _{DD2} (Q)	709	886	1152	μA	3.3V Input signal

π 122M1x Quiescent Supply Current @ 5V _{DC} Supply	I _{DD1} (Q)	419	524	681	μ A	0V Input signal	
	I _{DD2} (Q)	419	524	681	μ A	0V Input signal	
	I _{DD1} (Q)	436	545	709	μ A	5V Input signal	
	I _{DD2} (Q)	436	545	709	μ A	5V Input signal	
	@ 3.3V _{DC} Supply	I _{DD1} (Q)	414	518	673	μ A	0V Input signal
		I _{DD2} (Q)	414	518	673	μ A	0V Input signal
		I _{DD1} (Q)	408	510	663	μ A	3.3V Input signal
		I _{DD2} (Q)	408	510	663	μ A	3.3V Input signal

Table 7. Total Supply Current vs. Data Throughput (C_L = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	150 Kbps			1 Mbps			10 Mbps			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
π 120M1x Supply Current @ 5V _{DC}	I _{DD1}	0.14	0.21		0.15	0.22		0.24	0.36		mA	
	I _{DD2}	0.95	1.43		1.02	1.52		1.76	2.63		mA	
	@ 3.3V _{DC}	I _{DD1}	0.11	0.17		0.12	0.17		0.18	0.27		mA
		I _{DD2}	0.93	1.40		0.97	1.46		1.43	2.14		mA
π 122M1x Supply Current @ 5V _{DC}	I _{DD1}	0.54	0.81		0.58	0.86		0.97	1.60		mA	
	I _{DD2}	0.54	0.81		0.58	0.86		0.97	1.60		mA	
	@ 3.3V _{DC}	I _{DD1}	0.52	0.78		0.54	0.81		0.77	1.20		mA
		I _{DD2}	0.52	0.78		0.54	0.81		0.77	1.20		mA

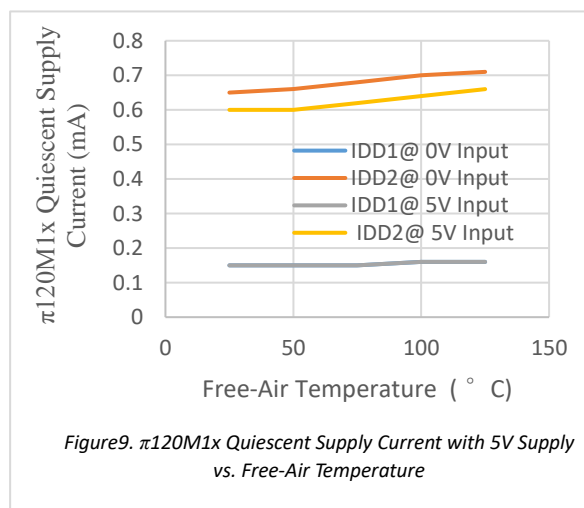
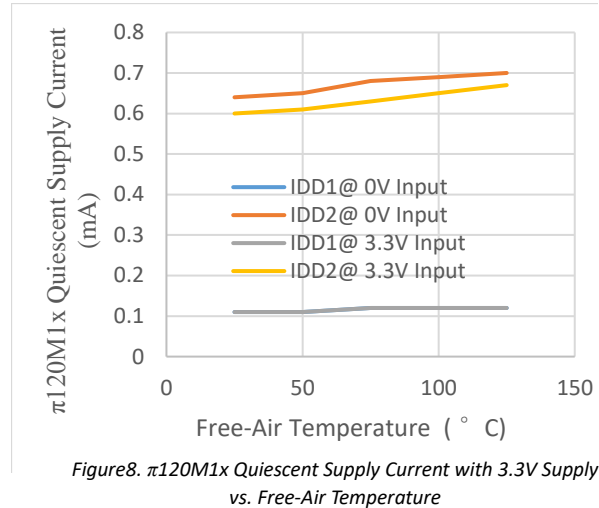
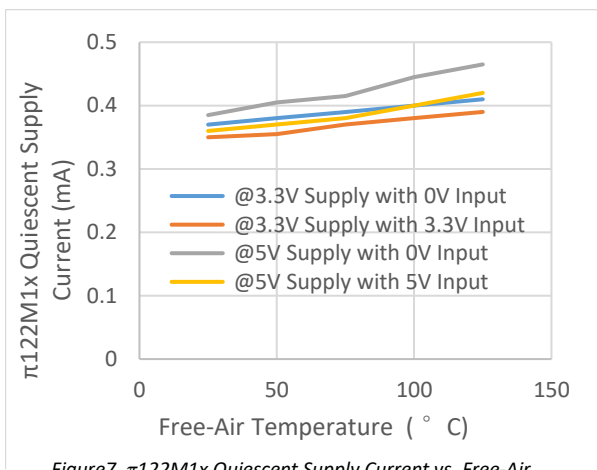
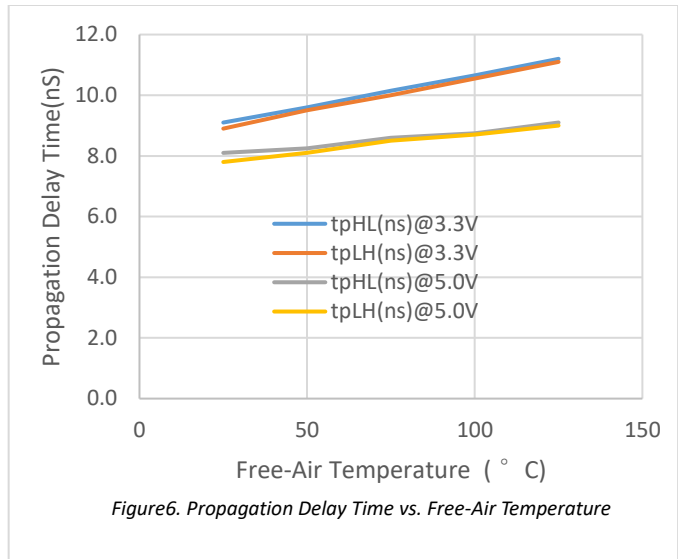
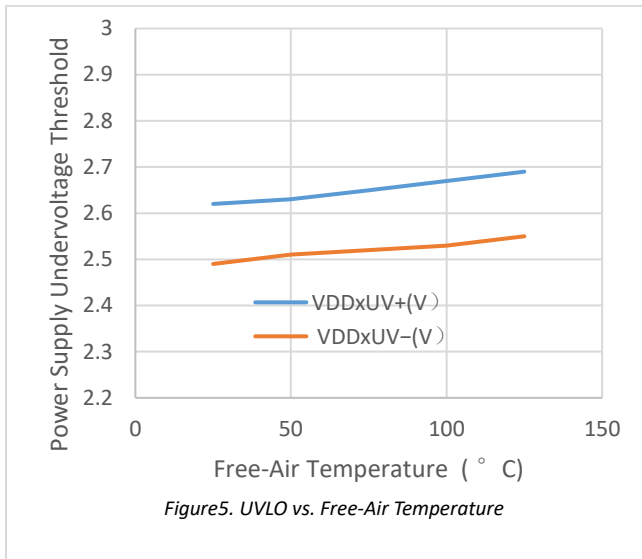
PACKAGE CHARACTERISTICS**Table 8. Package Characteristics**

Parameter	Symbol	Typical Value	Unit	Test Conditions/Comments
		π 12xM1x		
Resistance (Input to Output) ¹	R _{I-O}	10 ¹¹	Ω	
Capacitance (Input to Output) ¹	C _{I-O}	0.6	pF	@1MHz
Input Capacitance ²	C _I	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	100	°C/W	Thermocouple located at center of package underside

Notes:

¹The device is considered a 2-terminal device; DFN Pin 1 - Pin 4 are shorted together as the one terminal, and DFN Pin 5 - Pin 8 are shorted together as the other terminal.

²Testing from the input signal pin to ground.



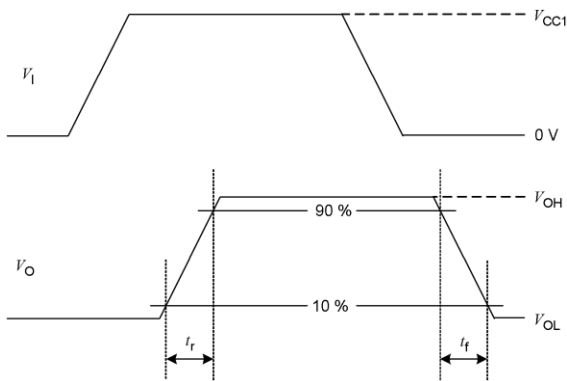


Figure10. Transition time waveform measurement

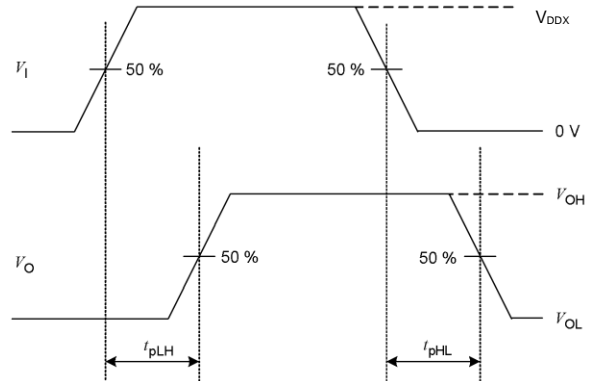


Figure11. Propagation delay time waveform measurement



2Pai Semi

APPLICATIONS INFORMATION

OVERVIEW

The $\pi 1xxxxx$ are 2PaiSemi digital isolators product family based on 2PaiSEMI unique **iDivider** technology. Intelligent voltage **Divider** technology (**iDivider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, **iDivider** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using matured standard semiconductor CMOS technology and the innovative **iDivider** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The $\pi 1xxxxx$ isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The $\pi 120M1x/\pi 122M1x$ are the outstanding 10 Mbps dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic.

The $\pi 120M1x/\pi 122M1x$ have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2 . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF . To enhance the robustness of a design,

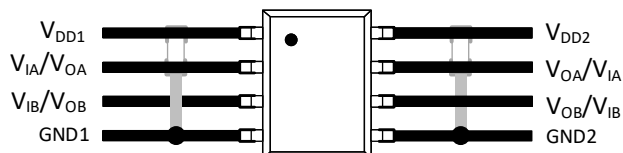


Figure12.Recommended Printed Circuit Board Layout

the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of $\pi 1xxxxx$ isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The common-mode pulse generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to $\pi 1xxxxx$ isolator coupler under measurement. The common-mode pulse is applied between one side ground GND_1 and the other side ground GND_2 of $\pi 1xxxxx$ isolator and shall be capable of providing positive transients as well as negative transients.

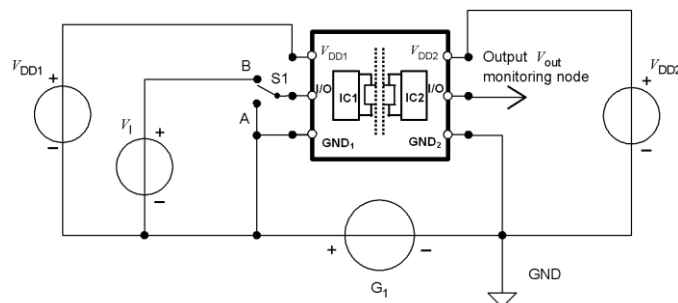
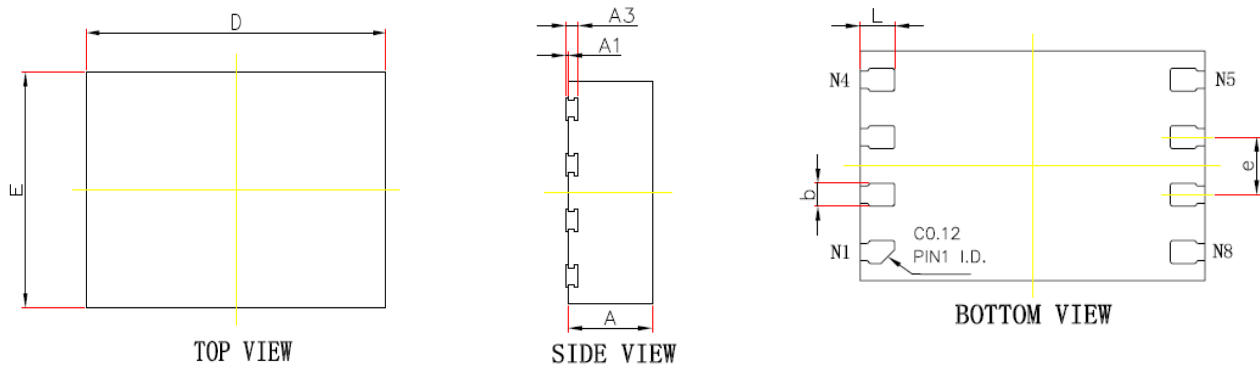


Figure13. Common-mode transient immunity (CMTI) measurement

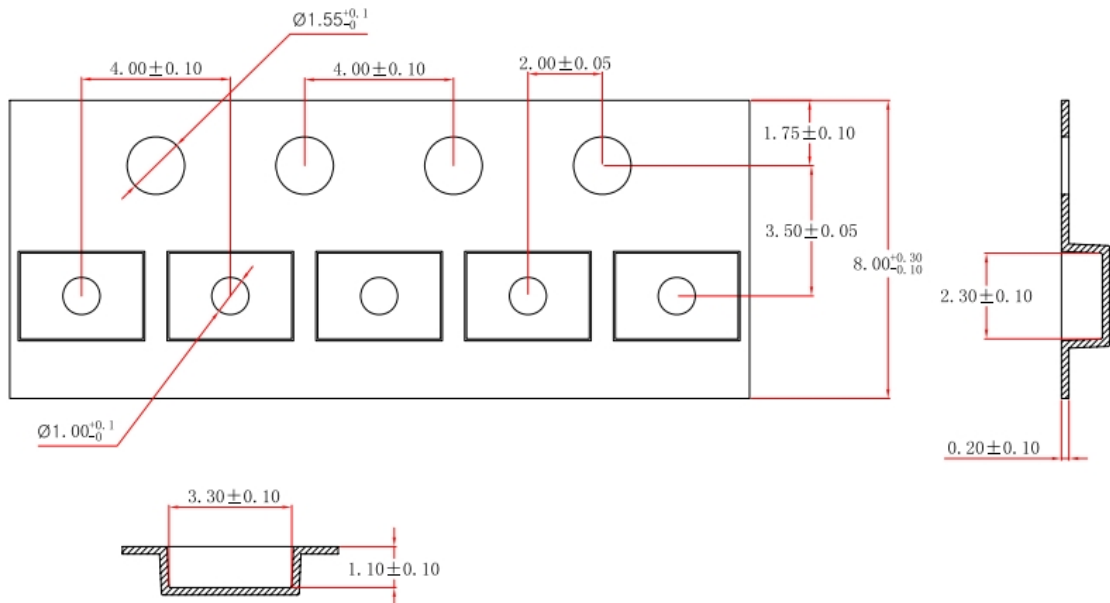
OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	-0.004	0.046	0.000	0.002
A3	0.110REF.		0.004REF.	
D	2.900	3.100	0.114	0.122
E	1.900	2.100	0.075	0.083
b	0.150	0.250	0.006	0.010
e	0.500BSC.		0.020BSC.	
L	0.250	0.350	0.010	0.014

Figure14. 8-PIN DFN Outline Package (3mm*2mm)

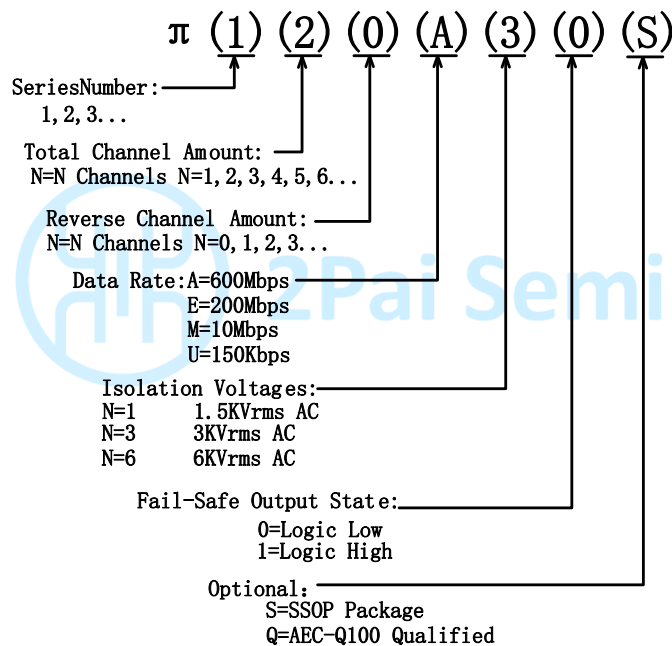
REEL INFORMATION



ORDERING GUIDE

Model Name		Temperature Range	No. of Inputs, V _{DD1} Side	No. of Inputs, V _{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
π 120M11	Pai120M11	-40°C to +125°C	2	0	1.5	High	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel
π 120M10	Pai120M10	-40°C to +125°C	2	0	1.5	Low	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel
π 122M11	Pai122M11	-40°C to +125°C	1	1	1.5	High	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel
π 122M10	Pai122M10	-40°C to +125°C	1	1	1.5	Low	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel

PART NUMBER NAMED RULE



Notes:

Pai12xxxx is equals to π 12xxxx in the customer BOM

REVISION HISTORY

Revision	Updated	Date	Page	Change Record
1	Jason	2019/02/18	All	Initial version
2	Jason	2019/04/24	P1,P7, P9	P1: Changed the address from 'Room 19307, Building 8, No.498, GuoShoujing Road' to 'Room 308-309, No.22, Boxia Road'; Add iDivider technology description in General Description. P7: Add iDivider technology description in overview. P9: Add character 'S' and 'Q' in part number named rule
3	Devin	2019/09/08	P1	P1: Changed propagation delay for 5V from 7.5ns to 8ns. Changed CMTI from 50KV/us to 75KV/us. Changed ESD(HBM) from 7KV to 8KV.