2Pai Semi

Enhanced ESD, 1.5kV rms 200Mbps Single-Channel Digital Isolator

Data Sheet **π110E1**

FEATURES

- **Ultra low power consumption (1Mbps):**
  - **0.75mA/Channel**
- **High data rate:**
  - **π110E1x: 200Mbps**
- **High common-mode transient immunity: 75 kV/μs typical**
- **High robustness to radiated and conducted noise**
- **Low propagation delay:**
  - **8 ns typical for 5 V operation**
  - **9 ns typical for 3.3 V operation**
- **Isolation voltages:**
  - **π110E1x: AC 1500Vrms**
- **High ESD rating:**
  - **ESDA/JEDEC JS-001-2017**
  - **Human body model (HBM) ±8kV, all pins**
- **3 V to 5.5 V level translation**
- **Wide temperature range: -40°C to 125°C**
- **8-PIN, RoHS-compliant, DFN package(3mm*2mm)**

APPLICATIONS

- **General-purpose multichannel isolation**
- **Industrial field bus isolation**

GENERAL DESCRIPTION

The π1xxxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSEMI ***i*Divider** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***i*Divider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

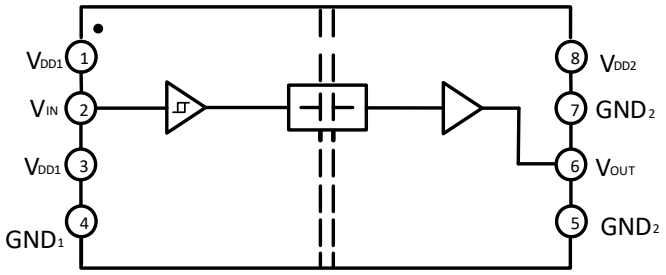

Figure1. π110E1x functional Block Diagram

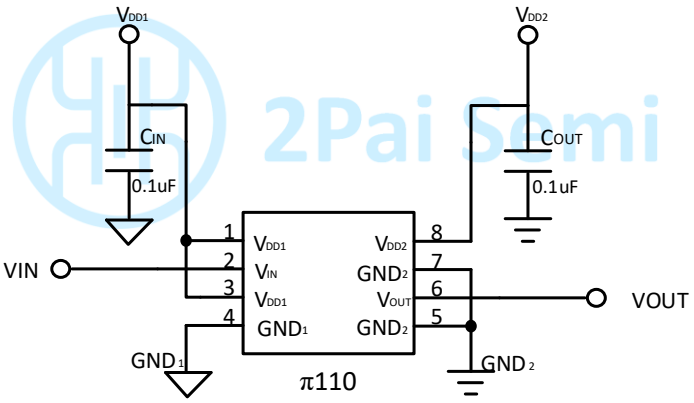

Figure2. π110E1x Typical Application Circuit

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PIN CONFIGURATIONS AND FUNCTIONS

π110E1x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IN}	Logic Input.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OUT}	Logic Output.
7	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

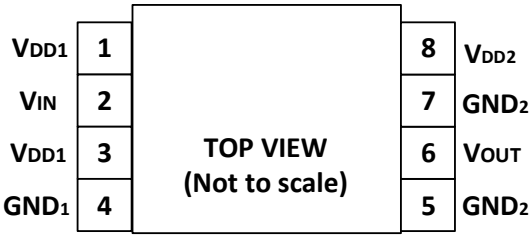


Figure3. π110E1X Pin Configuration

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 1. Absolute Maximum Ratings[3]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Average Output Current per Pin Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients Immunity[2]	−150 kV/µs to +150 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[2] See Figure11 for Common-mode transient immunity (CMTI) measurement.

[3] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
High Level Input Signal Voltage	V_{IH}	0.7*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Maximum Data Rate		0		200	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 3. π110xxx Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:

[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means V_{DDx}≥ 2.9 V

[3] Unpowered means V_{DDx} < 2.3V

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 1us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 4. Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			5	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		200			Mbps	Within PWD limit
Propagation Delay Time[1]	t_{pHL}, t_{pLH}	5.5	8	12.5	ns	The different time between 50% input signal to 50% output signal @ 5V_{DC} supply
		6.5	9	13.5	ns	@ 3.3V_{DC} supply
Pulse Width Distortion	PWD	0	0.3	0.8	ns	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	0.3	0.8	ns	@ 3.3V_{DC} supply
Output Signal Rise/Fall Time	t_r/t_f		1.5		ns	10% to 90% signal terminated 1MΩ//14pF oscilloscope input impedance， See figure9.
Rated Dielectric Insulation Voltage	V_{ISO}	1.5			kV rms	1-minute duration
Common-Mode Transient Immunity[3]	CMTI		75		kV/μs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000 V
ESD（HBM - Human body model）	ESD		±8kV		kV	All pins

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See figure 9.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See Figure11 for Common-mode transient immunity (CMTI) measurement.

Table 5. DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		0.6*V_{DDx}[1]	0.7*V_{DDx}[1]	V	

Falling Input Signal Voltage Threshold	V_{IT-}	0.3* V_{DDX}[1]	0.4* V_{DDX}[1]		V	
High Level Output Voltage	V_{OH} [1]	V_{DDx} – 0.1	V_{DDx}		V	−20 µA output current
		V_{DDx} – 0.2	V_{DDx} – 0.1		V	−2 mA output current
Low Level Output Voltage	V_{OL}		0	0.1	V	20 µA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I_{IN}	−10	0.5	10	µA	0 V ⩽ Signal voltage ⩽ V_{DDX}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.65	2.9	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.3	2.5	2.75	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 6. Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
π110E1x Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$	61	76	99	µA	0V Input signal
	$I_{DD2 (Q)}$	468	586	761	µA	0V Input signal
	$I_{DD1 (Q)}$	152	190	247	µA	5V Input signal
	$I_{DD2 (Q)}$	443	554	720	µA	5V Input signal
@ 3.3V_{DC} Supply	$I_{DD1 (Q)}$	60	75	98	µA	0V Input signal
	$I_{DD2 (Q)}$	463	579	753	µA	0V Input signal
	$I_{DD1 (Q)}$	112	140	182	µA	3.3V Input signal
	$I_{DD2 (Q)}$	425	532	691	µA	3.3V Input signal

Table 7. Total Supply Current vs. Data Throughput (C_L = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	150 Kbps			10 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
π110E1x Supply Current @ 5V_{DC}	I_{DD1}		0.12	0.18		0.20	0.30		1.01	1.52	mA
	I_{DD2}		0.57	0.86		1.06	1.58		4.48	6.71	mA
@ 3.3V_{DC}	I_{DD1}		0.10	0.15		0.16	0.24		0.61	0.92	mA
	I_{DD2}		0.56	0.84		0.86	1.29		2.93	4.39	mA

PACKAGE CHARACTERISTICS

Table 8. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{11}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		0.6		pF	@1MHz
Input Capacitance[2]	C_I		3.0		pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}		100		°C/W	Thermocouple located at center of package underside

Notes:
[1]The device is considered a 2-terminal device; DFN Pin 1 - Pin 4 are shorted together as the one terminal, and DFN Pin 5 - Pin 8 are shorted together as the other terminal.
[2]Testing from the input signal pin to ground.

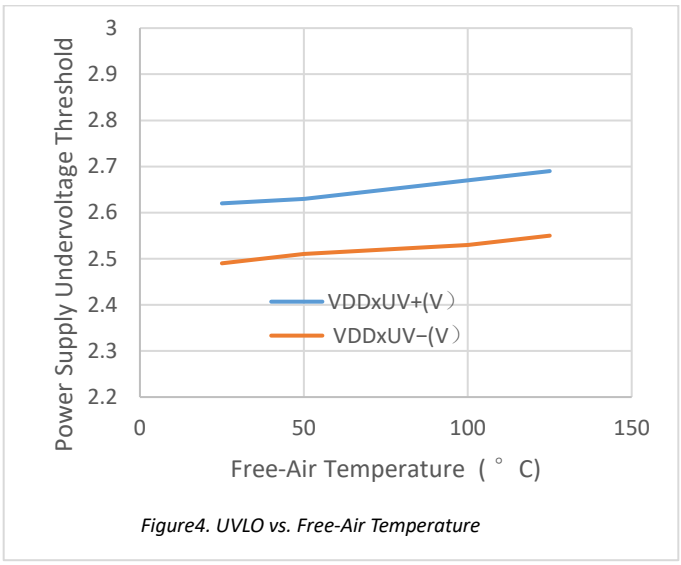


Figure4. UVLO vs. Free-Air Temperature

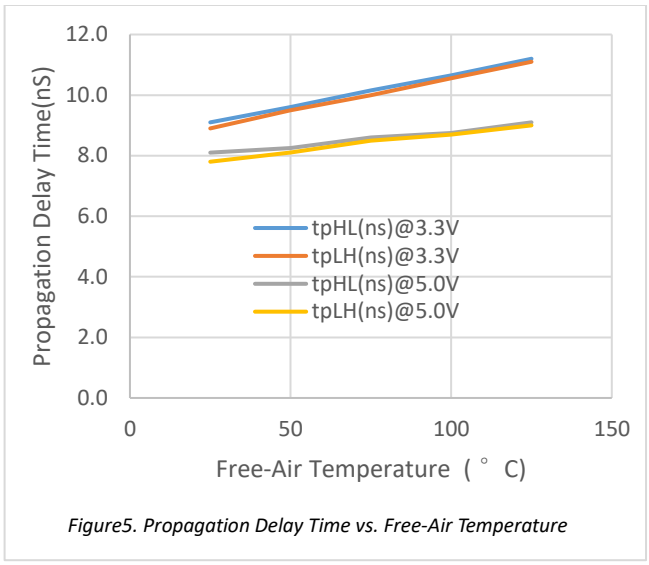


Figure5. Propagation Delay Time vs. Free-Air Temperature

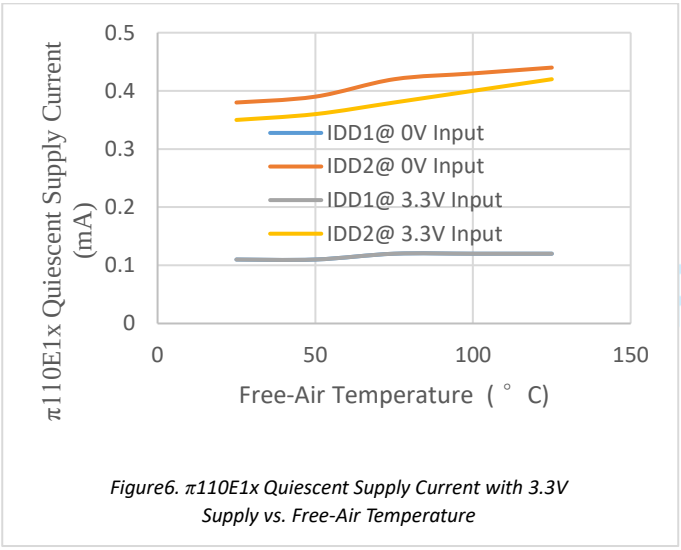


Figure6. π110E1x Quiescent Supply Current with 3.3V Supply vs. Free-Air Temperature

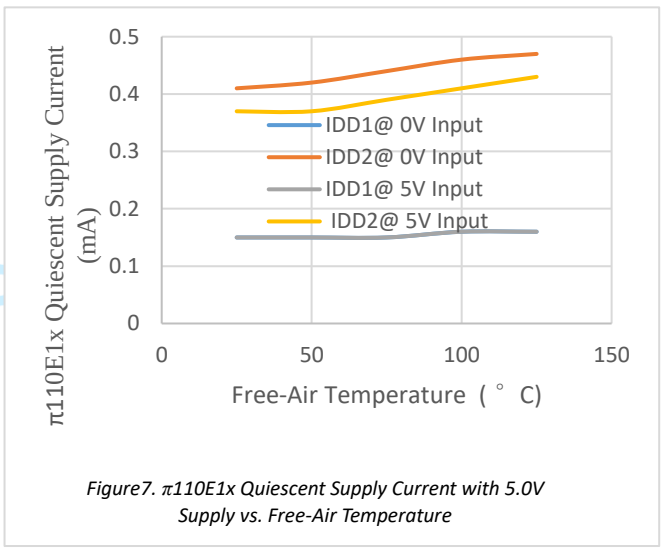


Figure7. π110E1x Quiescent Supply Current with 5.0V Supply vs. Free-Air Temperature

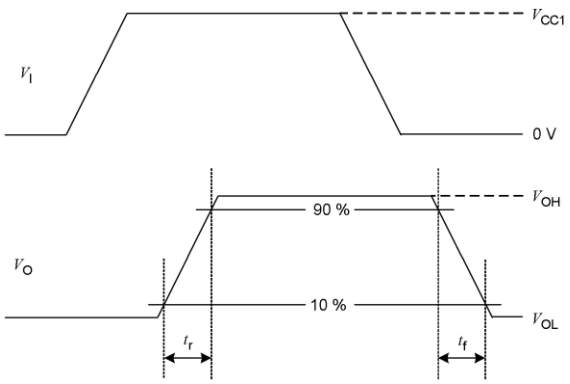


Figure8. Transition time waveform measurement

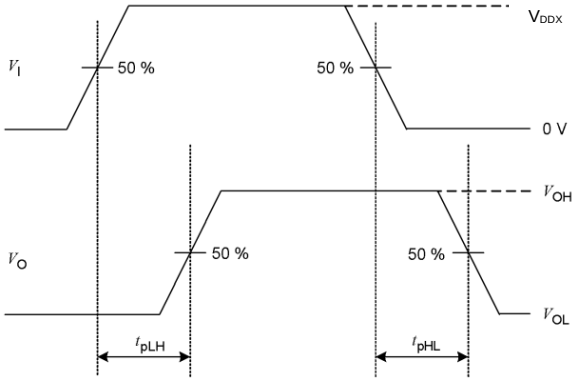


Figure9. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The π1xxxxx are 2PaiSemi digital isolators product family based on 2PaiSEMI unique ***i*Divider** technology. Intelligent voltage **Divider** technology (***i*Divider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***i*Divider** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***i*Divider** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The π110E1x are the outstanding 200 Mbps single-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic.

The π110E1x have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

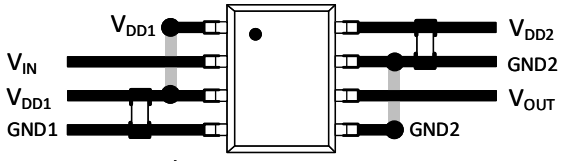


Figure10.Recommended Printed Circuit Board Layout

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The common-mode pulse generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

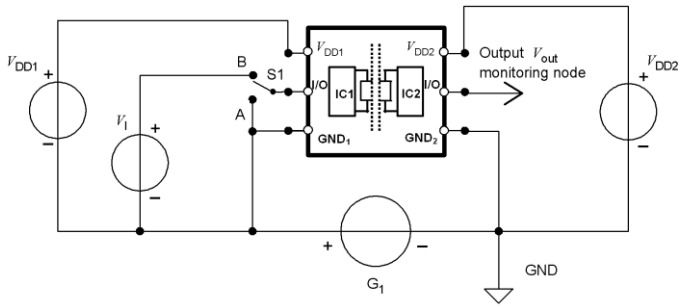
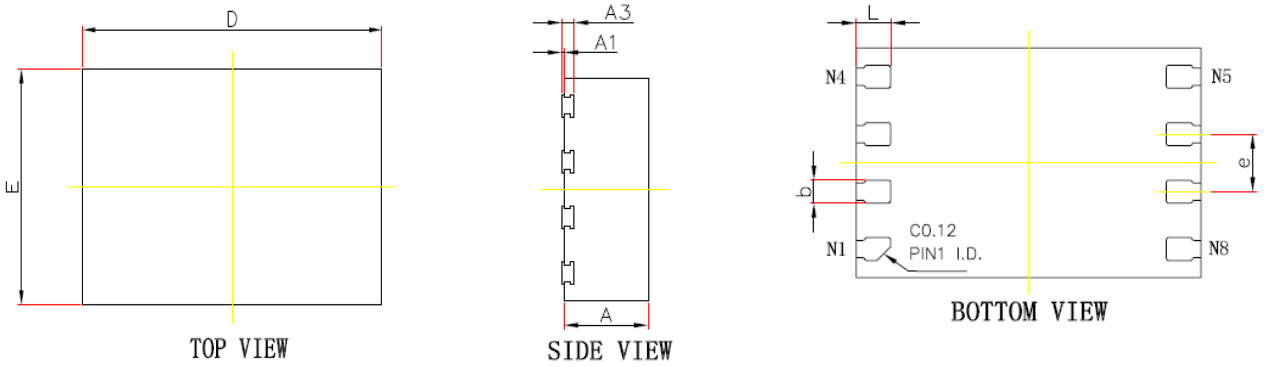


Figure11. Common-mode transient immunity (CMTI) measurement

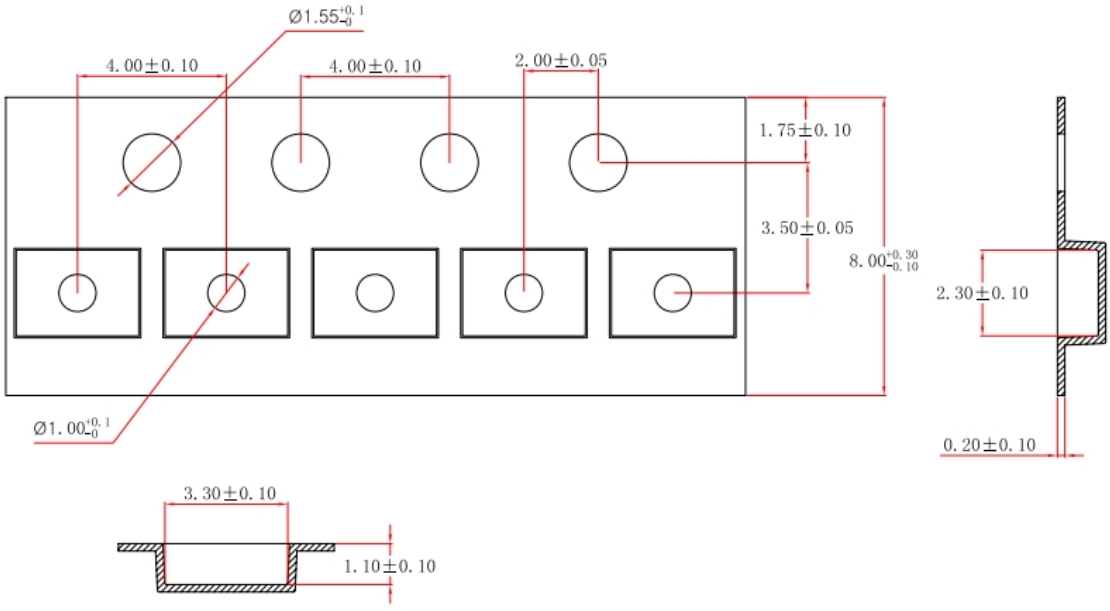
OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	-0.004	0.046	0.000	0.002
A3	0.110REF.		0.004REF.	
D	2.900	3.100	0.114	0.122
E	1.900	2.100	0.075	0.083
b	0.150	0.250	0.006	0.010
e	0.500BSC.		0.020BSC.	
L	0.250	0.350	0.010	0.014

*Figure12. 8-PIN DFN Outline Package（3mm*2mm）*

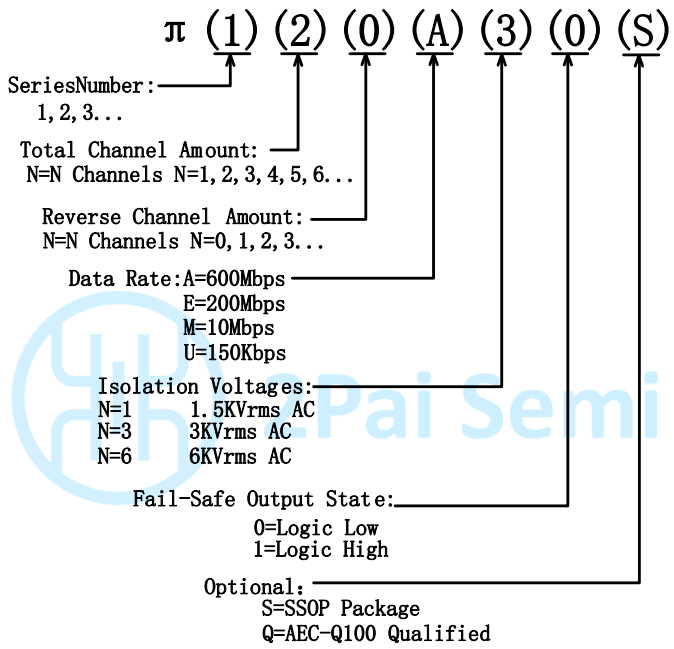
REEL INFORMATION



ORDERING GUIDE

Model Name		Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
π110E11	Pai110E11	−40°C to +125°C	1	0	1.5	High	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel
π110E10	Pai110E10	−40°C to +125°C	1	0	1.5	Low	8-P DFN 2mm*3mm	8-P-DFN	4000 per reel

PART NUMBER NAMED RULE



Notes:
Pai12xxxx is equals to π12xxxx in the customer BOM

REVISION HISTORY

Revision	Updated	Date	Page	Change Record
1	Jason	2019/02/18	All	Initial version
2	Jason	2019/04/24	P1,P6,P8	P1: Changed the address from 'Room 19307, Building 8, No.498, GuoShouJing Road' to 'Room 308-309, No.22, Boxia Road' ; Add ***i*Divider** technology description in General Description. P6: Add ***i*Divider** technology description in overview. P8: Add character 'S' and 'Q' in part number named rule
3	Devin	2019/09/08	P1	P1: Changed propagation delay for 5V from 7.5ns to 8ns. Changed CMTI from 50KV/us to 75KV/us. Changed ESD(HBM) from 7KV to 8KV.